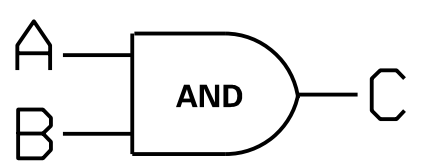
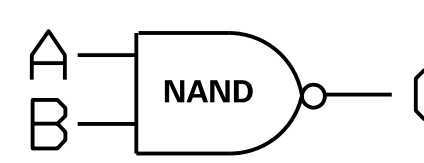


# LOGIC GATE

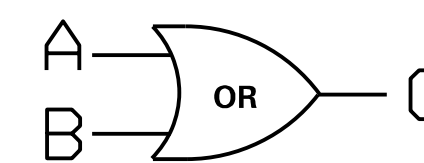
## TRUTH TABLE

AND GATE		
		
INPUT		OUT
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

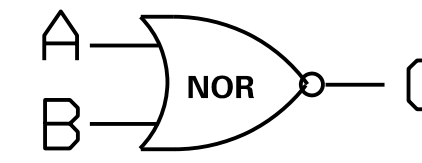
• OUTPUT IS 1 WHEN ALL INPUT IS 1

NAND GATE		
		
INPUT		OUT
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

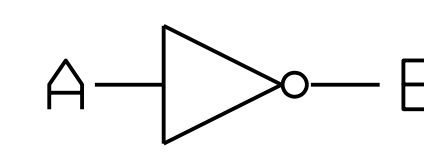
• OUTPUT IS 0 WHEN ALL INPUT IS 0

OR GATE		
		
INPUT		OUT
A	B	C
0	0	0
0	1	1
1	0	1
1	1	1


• OUTPUT IS 1 WHEN EITHER INPUT IS 1


NOR GATE		
		
INPUT		OUT
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

• OUTPUT IS 1 WHEN NONE INPUT IS 1

NOT GATE		
		
INPUT	A	OUT
B		
	0	1
	1	0

• OUTPUT IS REVERSE OF INPUT

ON-DELAY	
	
XX SECOND AFTER A=1 THAN B=1	

OFF-DELAY	
	
XX SECOND AFTER A=0 THAN B=0	

INPUT OR OUTPUT LEVEL

LEVEL 1 = 12 VOLTS OR 24 VOLTS

LEVEL 0 = 0 VOLT ( TO GROUND )