

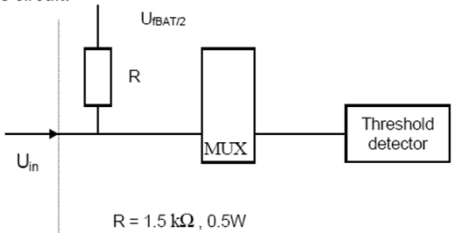
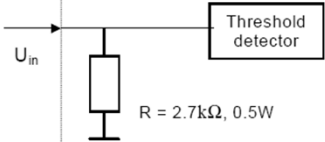
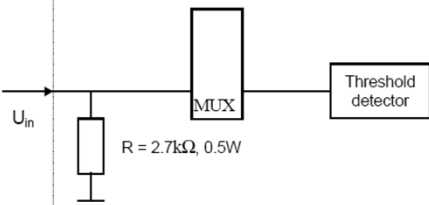
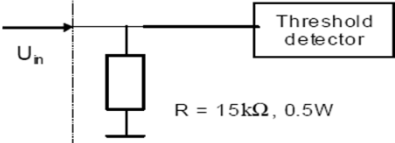
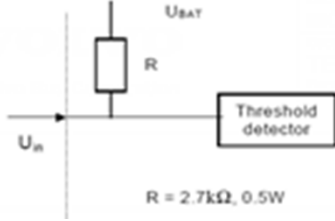
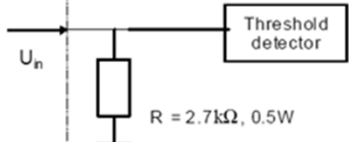
Wiring diagram pages list

Pin configuration MCM

Signal ID	J1 pin	Interface type	Input / Output	Description	Signal ID	J1 pin	Interface type	Input / Output	Description
A1	1	CAN0 High	Bus	Maximum speed 1Mbps/wake	B1	1	Type 1	In	LDI, HDI
A2	2	CAN0 Low	Bus	Maximum speed 1Mbps/wake	B2	2	Type 1	In	LDI, HDI, Failure mode
A3	3	Type 7	Out	LDO, Failure mode	B3	3	Type 2	In	HDI
A4	4	Type 7	Out	LDO	B4	4	Type 4a	In	HDI, Interrupt/Wake
A5	5	Type 7	Out	LDO	B5	5	Type 3	In	LDI, Interrupt/Wake
A6	6	Type 8	Out	LDO	B6	6	Type 4a	In	HDI Failure mode, Interrupt/Wake
A7	7	Type 8	Out	LDO	B7	7	RS232 TxD	Bus	Maximum speed 115,2kbps
A8	8	GND	In		B8	8	RS232 RxD	Bus	Maximum speed 115,2kbps
A9	9	Vbat	In		B9	9	Type 1	In	LDI, HDI
A10	10	Type 8	Out	LDO	B10	10	Type 1	In	LDI, HDI
A11	11	Type 10	Out	HDO	B11	11	Type 1	In	LDI, HDI
A12	12	Type 9B	Out	HDO	B12	12	RS232 GND	In	
A13	13	Type 9B	Out	HDO	B13	13	Type 1	In	LDI, HDI
A14	14	Type 9A	Out	HDO	B14	14	Type 1	In	LDI, HDI
A15	15	Type 9A	Out	HDO	B15	15	Type 4B	In	Interrupt/Wake
A16	16	Type 9A	Out	HDO, Failure mode	B16	16	Type 1	In	LDI, HDI
A17	17	Type 10	Out	HDO, Failure mode	B17	17	Type 1	In	LDI, HDI
A18	18	Type 9A	Out	HDO	B18	18	GND	In	
A19	19	Type 13	Out	C30	B19	19	MasterID Supply	In	
A20	20	Network ID 1	In		B20	20	NC		
A21	21	Network ID 2	In		B21	21	Type 1	In	LDI, HDI
A22	22	EOL enable	In		B22	22	Type 1	In	LDI, HDI
A23	23	Network ID 3	In		B23	23	Type 1	In	LDI, HDI
A24	24	Type 11	Out	HLDO	B24	24	RS232 CTS	In	
A25	25	Type 11	Out	HLDO	B25	25	Type 6	In	HAI
A26	26	Type 5	In	HDI	B26	26	Type 6	In	HAI
A27	27	CAN2 High	Bus	Maximum speed 1Mbps/wake	B27	27	RS232 RTS	Out	
A28	28	CAN2 Low	Bus	Maximum speed 1Mbps/wake	B28	28	Type 12	Out	HDO 5V
A29	29	GND	In		B29	29	Type 9	Out	HDO
A30	30	Vbat	In		B30	30	NC		

Wiring diagram pages list

Pin configuration MCM

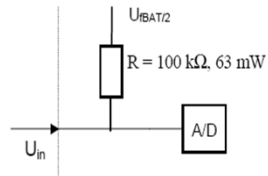
<p>Interface Circuit type 1, General purpose digital input The input can be used as a general input circuit interfacing to switches closing to ground and to battery (LDI/HDI). It can also be used to interface with resistive switches and sensors.</p> <p>DC model of this circuit:</p>  <p>$R = 1.5\text{ k}\Omega, 0.5\text{W}$</p>	<p>Input circuit type 4a, High side digital input, interrupt DC model of input circuit type 4. The input is used to interface with switches closing to battery voltage (HDI)</p>  <p>$R = 2.7\text{ k}\Omega, 0.5\text{W}$</p>
<p>Input circuit type 2, High side digital input DC model of input circuit type 2. The input is used to interface with switches closing to battery voltage (HDI).</p>  <p>$R = 2.7\text{ k}\Omega, 0.5\text{W}$</p>	<p>Input circuit type 4b, High side digital input, interrupt The input is used to wake up the CECM from sleep mode.</p>  <p>$R = 15\text{ k}\Omega, 0.5\text{W}$</p>
<p>Input circuit type 3, Low side digital input, interrupt DC model of input circuit type 3. The input is used to interface with switches closing to ground voltage (LDI).</p>  <p>$R = 2.7\text{ k}\Omega, 0.5\text{W}$</p>	<p>Input circuit type 5, High side digital input DC model of input circuit type 5. the inputs is used to interface with switches closing to battery voltage</p>  <p>$R = 2.7\text{ k}\Omega, 0.5\text{W}$</p>

Wiring diagram pages list

Pin configuration MCM

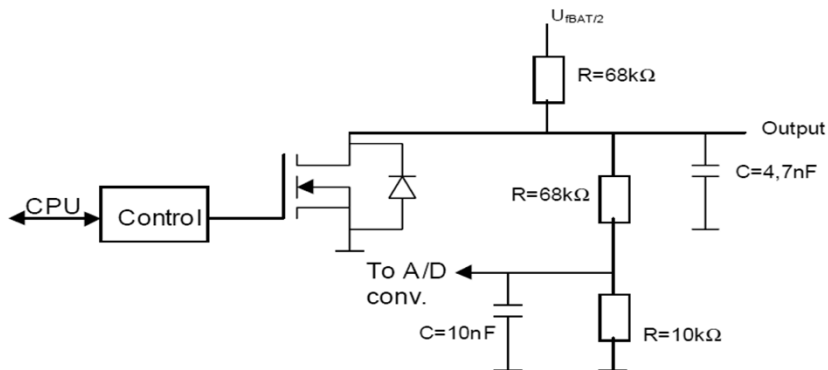
Input circuit type 6, Analogue input

The circuit is used as interface to variable voltage sources such as potentiometers and analogue sensors (HA1).
DC model of input circuit type 6:



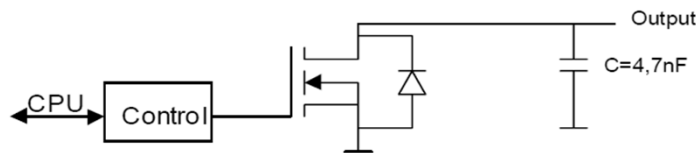
Output circuit type 7, LDO.

The figure below gives a schematic overview of the output type 7.



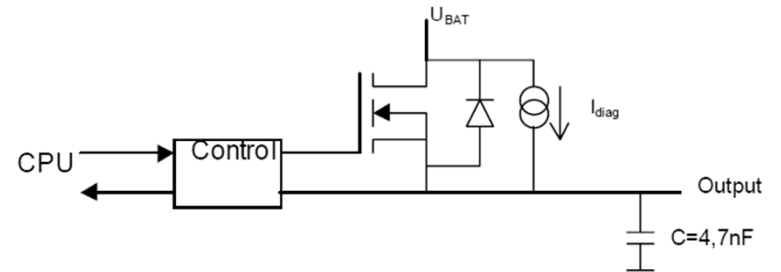
Output circuit type 8, LDO.

The figure below gives a schematic overview of the output type 8.



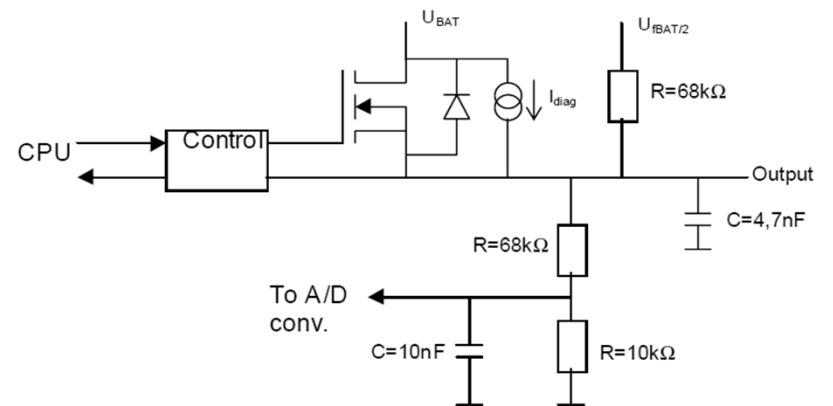
Output circuit type 9 a/b, HDO.

The figure below gives a schematic overview of the output type 9 a/b.



Output circuit type 10, HDO.

The figure below gives a schematic overview of the output type 10.

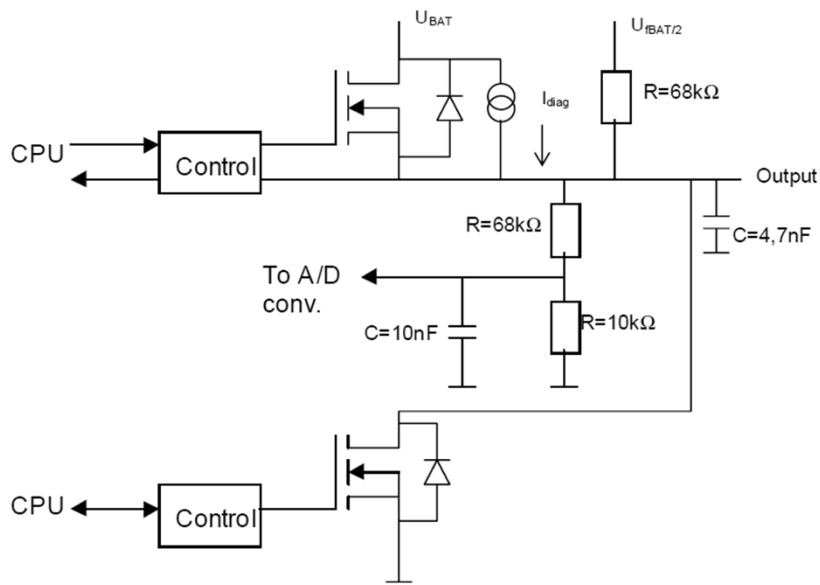


Wiring diagram pages list

Pin configuration MCM

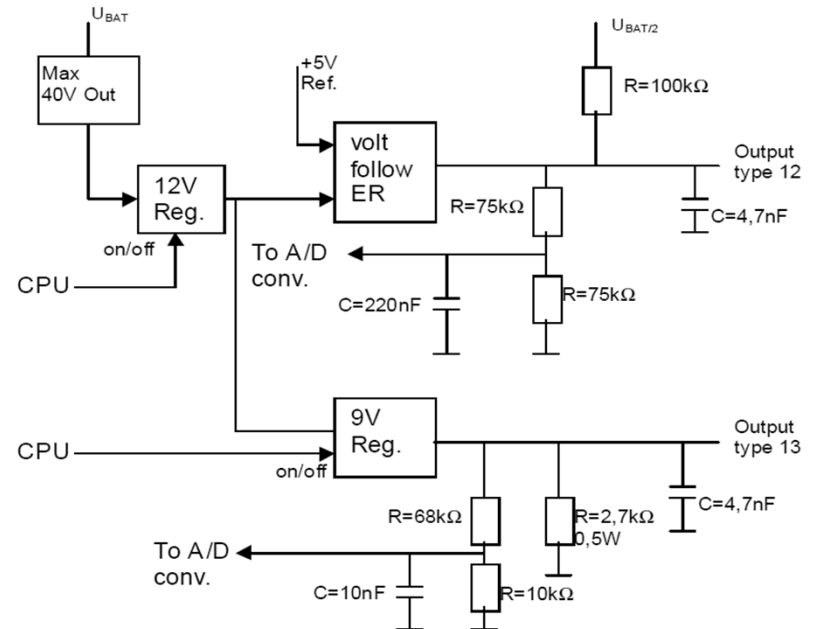
Output circuit type 11, L/HDO, PWM_{out}.

The figure below gives a schematic overview of the output type 11.



Output circuit type 12, HDO, 5V output and type 13, HDO.

The figure below gives a schematic overview of the output type 12 and 13.



Wiring diagram pages list

Pin configuration I/O-A+

Signal ID	J1 pin	Interface type	Input / Output	Description	Max current average	Max current peak	Signal ID	J1 pin	Interface type	Input / Output	Description	Max current average	Max current peak
J1-1	1	4c	Out	HDO, LDO, HLDO, HPO	1A	1A	J2-6	6	1a	In	HDI, LDI, HLDI, RAI	*	*
J1-2	2	1a, 1b, 1c	In	HDI, LDI, HLDI, RES, RES32K, AI5V, RAI, CNTR1, CNTR2	*	*	J2-7	7	1a	In	HDI, LDI, HLDI, RAI	*	*
J1-3	3	4c	Out	HDO, LDO, HLDO, HPO	1A	1A	J2-8	8	1a	In	HDI, LDI, HLDI, RAI	*	*
J1-4	4	4c	Out	HDO, LDO, HLDO, HPO	1A	1A	J2-9	9	1a	In	HDI, LDI, HLDI, RAI	*	*
J1-5	5	1a, 1b, 1c	In	HDI, LDI, HLDI, RES, RES32K, AI5V, RAI, CNTR1, CNTR2	*	*	J2-10	10	1a	In	HDI, LDI, HLDI, RAI	*	*
J1-6	6	GND	In	Analog GND	*	*	J2-11	11	1a	In	HDI, LDI, HLDI, RAI	*	*
J1-7	7	4c	Out	HDO, LDO, HLDO, HPO	1A	1A	J2-12	12	1a	In	HDI, LDI, HLDI, RAI	*	*
J1-8	8	Network ID	In	NI	*	*	J2-13	13	1a	In	HDI, LDI, HLDI, RAI	*	*
J1-9	9	Network ID	In	NI	*	*	J2-14	14	GND	Out	Analog GND	*	*
J1-10	10	4c	Out	HDO, LDO, HLDO, HPO	1A	1A	J2-15	15	3a, 5	Out	HDO, REFCTL	50mA	50mA
J1-11	11	Network ID	In	NI	*	*							
J1-12	12	Network ID	In	NI	*	*							
J1-13	13	4c	Out	HDO, LDO, HLDO, HPO									
J1-14	14	Network ID	In	NI	*	*							
J1-15	15	Network ID	In	NI	*	*							
J1-16	16	4b	Out	HDO, LDO, HLDO, HPO, LPO									
J1-17	17	1a, 1c	In	HDI, LDI, HLDI, RES, RES32K, AI5V, RAI, CNTR1	*	*							
J1-18	18	GND	In	GND	*	*							
J1-19	19	4b	Out	HDO, LDO, HLDO, HPO, LPO	1A	1A							
J1-20	20	1a, 1c	In	HDI, LDI, HLDI, RES, RES32K, AI5V, RAI	*	*							
J1-21	21	1a	In	HDI, LDI, HLDI, RES, RES32K, AI5V, RAI	*	*							

Wiring diagram pages list

Pin configuration I/O-B+

Signal ID	J1 pin	Interface type	Input / Output	Description	Max current average	Max current peak	Signal ID	J1 pin	Interface type	Input / Output	Description	Max current average	Max current peak
J1-1	1	4d	Out	HDO, LDO, HLDO, HPO, LPO	16A	20A	J2-1	1	4d	Out	HDO, LDO, HLDO, HPO, LPO	10A	20A
J1-2	2	*	*	*	*	*	J2-2	2	GND	*	*	*	*
J1-3	3	4d	out	HDO, LDO, HLDO, HPO, LPO	16A	20A	J2-3	3	GND	*	*	*	*
J1-4	4	3c	Out	HDO	10A	20A	J2-4	4	4d	Out	HDO, LDO, HLDO, HPO, LPO	10A	20A
J1-5	5	GND	*	*	*	*	J2-5	5	1a, 2b, 6	In	HDI, LDI, HLDI, RAI, AI5V, RES, RES32K, CNTR, wake-up	*	*
J1-6	6	GND	Out	Analogue GND	*	*	J2-6	6	1a, 2b, 6	In	HDI, LDI, HLDI, RAI, AI5V, RES, RES32K, CNTR, wake-up	*	*
J1-7	7	3c	Out	HDO	10A	20A	J2-7	7	4c	In	HDO, LDO, HLDO, HPO	10A	20A
J1-8	8	NI	*	*	*	*	J2-8	8	1a,1b,1c	In	HDI, LDI, HLDI, RAI, AI5V, RES, RES32K	*	*
J1-9	9	NI	*	*	*	*	J2-9	9	1a,1b,1c	In	HDI, LDI, HLDI, RAI, AI5V, RES, RES32K	*	*
J1-10	10	3c	Out	HDO	10A	20A	J2-10	10	4c	Out	HDO, LDO, HLDO, HPO	10A	20A
J1-11	11	NI	*	*	*	*	J2-11	11	1b, 1c	In	AI5V, RES, RES32K	*	*
J1-12	12	NI	*	*	*	*	J2-12	12	1b, 1c	In	AI5V, RES, RES32K	*	*
J1-13	13	3c	Out	HDO	10A	20A	J2-13	13	3e	Out	HDO, LDO, HLDO	10A	20A
J1-14	14	NI	*	*	*	*	J2-14	14	GND	Out	Analogue GND	*	*
J1-15	15	NI	*	*	*	*	J2-15	15	5	Out	REFMEA	< 50 mA	*
J1-16	16	3c	Out	HDO	10A	20A							
J1-17	17	GND	*	*	*	*							
J1-18	18	GND	*	*	*	*							
J1-19	19	3c	Out	HDO	10A	20A							
J1-20	20	1a	In	HDI, LDI, HLDI, RAI	*	*							
J1-21	21	1a	In	HDI, LDI, HLDI, RAI	*	*							

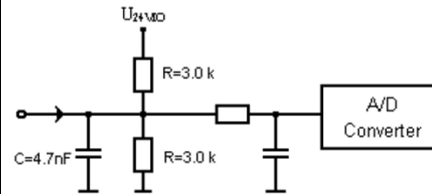
Wiring diagram pages list

Pin configuration I/O-A+ and I/O-B+

Interface circuit 1a

The input can be used for both digital and analogue signals that have U_{24VIO} as reference. The circuit shall sink 8 mA when connected to U_{24VIO} or source 8 mA when connected to GND. The input shall be converted from analog voltage to digital 10 bit resolution with scaling relative to U_{24VIO} . The input shall be regarded as a power line according to "Volvo Technical Regulation 15 79 908, EMC Requirements".

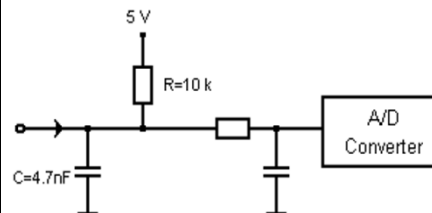
Model of the input circuit:



Interface circuit 1b

The input is used for resistive sensors. The circuit shall supply 5 V through a resistor of 10 kΩ. When used to measure temperature, the output current to the sensor shall then be minimised to avoid internal power dissipation in the sensor.

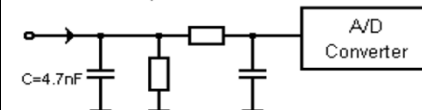
Model of the input circuit:



Interface circuit 1c

The input can be used for both digital and analogue signals. The total input resistance $R_{tot} = R // R_{A/D}$, shall be $100 \text{ k}\Omega < R_{tot} < 500 \text{ k}\Omega$.

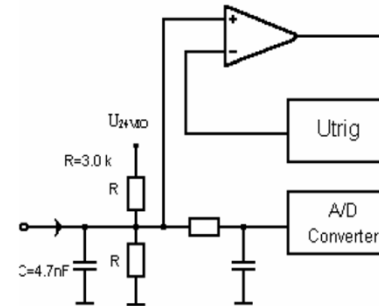
Model of the input circuit:



Interface circuit 2b

Pulse input circuit. The input can be used for both digital and analogue signals and as pulse counter input with fixed trigger level. The circuit shall sink or source 8 mA at $U_{24VIO} = 28 \text{ V}$ when connected to U_{24VIO} or GND.

Model of input circuit:



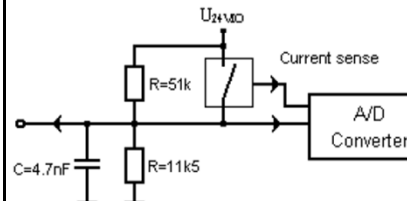
Interface circuit 3a

Model of high side output stage circuit same as interface circuit 3b in Chapter 2.3.1.5.2, but without PWM capability and no biasing resistors for open circuit detection.

Interface circuit 3c

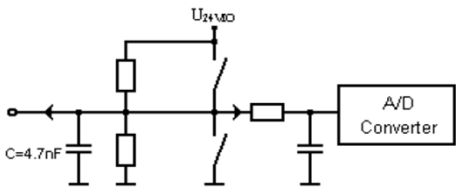
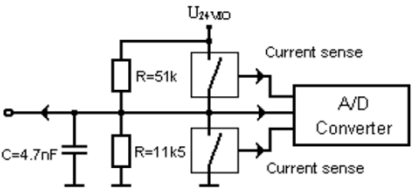
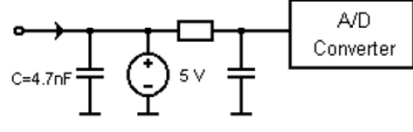
High side output circuit. The switch provides current sense signal to an A/D converter. To detect open circuit when the switch is open the interface shall sink approximately 2 mA when connected to $U_{24VIO} = 28 \text{ V}$ or source approximately 0.5 mA when connected to GND. The voltage shall be converted to digital 10 bit resolution with scaling relative to U_{24VIO} . The interface shall not be regarded as a power line according to "Volvo Technical Regulation 15 79 908, EMC Requirements".

Model of the output circuit:



Wiring diagram pages list

Pin configuration I/O-A+ and I/O-B+

<p>Interface circuit 3e Model of high side, low side output stage. This circuit is similar to circuit 4b but without PWM drive capabilities.</p>	<p>Interface circuit 4d Totem pole output stage may be used as high side, low side or high/low switch. Capable of low frequency PWM driving high side or low side switch but not both synchronously. Both switches provide current sense signal to an A/D converter. To detect open circuit when the switches are open the interface shall sink approximately 2 mA when connected to $U_{24VIO} = 28V$ or source approximately 0.5 mA when connected to GND. The voltage shall be converted to digital 10 bit resolution with scaling relative to U_{24VIO}. The interface shall not be regarded as a power line according to "Volvo Technical Regulation 15 79 908, EMC Requirements".</p>
<p>Interface circuit 4b Totem pole output stage may be used as high side, low side or high/low switch. Capable of low frequency PWM driving high side or low side switch but not both synchronously. Open circuit voltage shall be approximately $9,2 V / U_{24VIO=28V}$. When the switch is open the interface shall sink approximately 2 mA if connected to $U_{24VIO=28V}$ or source 0.5 mA when connected to GND. The voltage shall be converted to digital 10 bit resolution with scaling relative to U_{24VIO}. The interface shall not be regarded as a power line according to "Volvo Technical Regulation 15 79 908, EMC Requirements".</p> <p>Model of the output circuit:</p> 	<p>Model of the output circuit:</p> 
<p>Interface circuit 4c Model of high side, low side output stage. This circuit is similar to circuit 4b but without low side PWM drive capabilities.</p>	<p>Interface circuit 5 Model of a 5 V reference voltage supply for potentiometers and pressure sensors. Supply current 20 mA, current limited to < 50 mA.</p> <p>Model of the output circuit:</p> 
	<p>Interface circuit 6 The pin is used for interrupt the ECU. Same interface as circuit 1a. The application software can initiate the interrupt function. The pin is used for waking-up the ECU from sleep mode.</p>

Wiring diagram pages list

Radiator fans drive junction box

