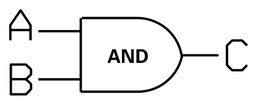
# LOGIC GATE

## TRUTH TABLE

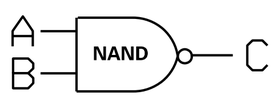
### AND GATE




| INPUT | | OUT |
|---|---|---|
| A | B | C |
| Ø | Ø | Ø |
| Ø | 1 | Ø |
| 1 | Ø | Ø |
| 1 | 1 | 1 |

*OUTPUT IS 1 WHEN ALL INPUT IS 1

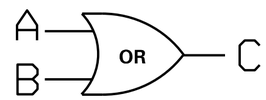
### NAND GATE




| INPUT | | OUT |
|---|---|---|
| A | B | C |
| Ø | Ø | 1 |
| Ø | 1 | 1 |
| 1 | Ø | 1 |
| 1 | 1 | Ø |

* OUTPUT IS Ø WHEN ALL INPUT IS Ø

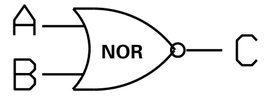
### OR GATE




| INPUT | | OUT |
|---|---|---|
| A | B | C |
| Ø | Ø | Ø |
| Ø | 1 | 1 |
| 1 | Ø | 1 |
| 1 | 1 | 1 |

* OUTPUT IS 1 WHEN EITHER INPUT IS 1

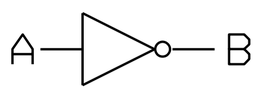
### NOR GATE




| INPUT | | OUT |
|---|---|---|
| A | B | C |
| Ø | Ø | 1 |
| Ø | 1 | Ø |
| 1 | Ø | Ø |
| 1 | 1 | Ø |

* OUTPUT IS 1 WHEN NONE INPUT IS 1

### NOT GATE




| INPUT | OUT |
|---|---|
| A | B |
| Ø | 1 |
| 1 | Ø |
| | |
| | |

* OUTPUT IS REVERSE OF INPUT

### ON-DELAY


XX SECOND
AFTER A=1
THAN B=1

### OFF-DELAY


XX SECOND
AFTER A=Ø
THAN B=Ø

INPUT OR OUTPUT LEVEL
LEVEL 1 = 12 VOLTS OR 24 VOLTS
LEVEL Ø = Ø VOLT (TO GROUND)